

REMARKS

The Examiner is thanked for discussing the application November 28, 2006, in an interview in which no agreement was reached.

It remains the applicant's position that the bootstrap circuit 15 of the Berringer, et al. patent is in the wrong place to heighten the input impedance of the output circuit 19 that generates an output voltage to a load 53 from an input voltage delayed by the delay circuit 21, 22.

The claimed output circuit has its input voltage delayed by the delay circuit. Therefore, in the Berringer, et al. patent, the output circuit must be on the right in Fig. 1, because the Action correctly finds the delay circuit 21, 22 in the middle. If the bootstrap circuit 15 heightens the input impedance from 38 as suggested in the interview, this would heighten the input impedance to the output circuit 19 on the right, but not of the output circuit, as claimed.

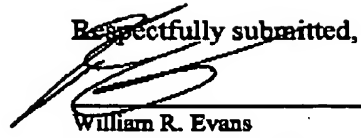
In any event, speculation on the Berringer, et al. circuit from the drawing is misplaced in view of the contrary description in column 5, lines 20-41, that its bootstrap circuit is an input current supply, which is not an impedance heightener, as claimed.

Nevertheless, new claims are presented above to try to described the differences of the invention more clearly.

An Information Disclosure Statement has also been filed.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,



William R. Evans
c/o Ladas & Parry LLP
26 West 61st Street
New York, New York 10023
Reg. No. 25858
Tel. No. (212) 708-1930